Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A microprocessor having a control register that is atomically modifiable by a privileged (kernel) instruction, the control register having bit fields, the microprocessor comprising:

a core, for receiving the privileged instruction and for atomically modifying the control register upon execution of the privileged instruction;

the privileged instruction comprising:

an opcode, for identifying the instruction as a privileged instruction;

a first operand, for specifying the control register as a register to be modified; and

a second operand, for specifying a location of a second register within the microprocessor, said second register containing a bit mask, said bit mask determining which of the bit fields within the control register are to be modified;

wherein said bit mask is used to atomically set or clear the bit fields in the control register;

whereby the bit fields in the control register are modified atomically by the privileged instruction.

2. (Original) The microprocessor as recited in claim 1 wherein the control register is not accessible when the microprocessor is executing unprivileged instructions.

3. (Original) The microprocessor as recited in claim 1 wherein the control register is directly modified by the privileged instruction without requiring the contents of the control register to first be moved to a general purpose (i.e., non-privileged) register.

4. (Original) The microprocessor as recited in claim 1 wherein the privileged instruction is executed when the microprocessor receives an interrupt signal.

5. (Original) The microprocessor as recited in claim 1 wherein the privileged instruction comprises:

a first instruction, for setting bit fields in the control register according to the contents of said bit mask; or

a second instruction, for clearing bit fields in the control register according to the contents of said bit mask.

6. (Original) The microprocessor as recited in claim 5 wherein said first instruction sets bit fields in the control register pertaining to corresponding bits that are set in said bit mask.

7. (Original) The microprocessor as recited in claim 5 wherein said second instruction clears bit fields in the control register pertaining to corresponding bits that are set in said bit mask.

8. (Original) The microprocessor as recited in claim 1 wherein said second register comprises a general purpose register.

9. (Original) The microprocessor as recited in claim 1 wherein the privileged instruction further comprises a field for specifying whether the bit fields in the control register are to be set or cleared according to said bit mask.

10. (Original) The microprocessor as recited in claim 1 wherein the control register comprises:

an interrupt mask bit field, said interrupt mask bit field having a plurality of bits, each of said plurality of bits for identifying interrupts received by the microprocessor.

11. (Original) The microprocessor as recited in claim 10 wherein by atomically clearing one of said plurality of bits using the privileged instruction, its corresponding interrupt is temporarily disabled.

12. (Currently amended) A method for atomically modifying ~~interrupt mask~~ bits within a privileged control register of a microprocessor, the method comprising:

providing a privileged instruction which instructs the microprocessor to atomically clear ~~particular~~ specified ones of the ~~interrupt mask~~ bits;

providing a ~~bit mask~~register, for specifying which of the particular ones of the ~~interrupt mask~~ bits are to be cleared; and

upon receipt of an interrupt by the microprocessor, atomically clearing the particular ones of the ~~interrupt mask~~ bits as specified by the ~~bit mask~~register.

13. (Currently amended) The method as recited in claim 12 wherein the ~~interrupt mask~~ bits specify which of a plurality of interrupts have been received by the microprocessor.

14. (Currently amended) The method as recited in claim 12 wherein the ~~interrupt mask~~ bits specify which of a plurality of interrupts are enabled.

15. (Currently amended) The method as recited in claim 12 wherein the privileged control register comprises a status register having a plurality of bit fields, including the ~~interrupt mask~~ bits.

16. (Currently amended) The method as recited in claim 12 wherein the privileged instruction comprises:

an opcode for designating the privileged instruction as privileged;

a first operand for designating the privileged control register as the register to be modified; and

a second operand for designating the location of the ~~bit mask~~register.

17. (Canceled)

18. (Original) A bit clear instruction for execution on a microprocessor having a privileged control register, the bit clear instruction executing on the microprocessor when the microprocessor receives an interrupt and when the microprocessor is in a privileged state, the bit clear instruction comprising:

a plurality of opcode bits for designating the bit clear instruction as a privileged instruction;

a plurality of first operand bits for designating the privileged control register as the register to be operated upon by the bit clear instruction; and

a plurality of second operand bits for designating a general purpose register as a register containing a bit mask, said bit mask specifying which of a plurality of bits within the privileged control register are to be cleared;

wherein when the bit clear instruction executes on the microprocessor, the plurality of bits within the privileged control register that are specified by said bit mask are cleared, atomically.

19. (Original) The bit clear instruction as recited in claim 18 wherein the privileged control register comprises a status register having an interrupt mask bit field.

20. (Original) A computer program product for use with a computing device, the computer program product comprising:

a computer usable medium, having computer readable program code embodied in said medium, for causing a microprocessor having a control register that is modifiable by a privileged instruction to be described, said computer readable program code comprising:

first program code for providing a core, for receiving the privileged instruction and for modifying the control register upon execution of the privileged instruction; and

second program code for providing the privileged instruction, the privileged instruction comprising:

an opcode, for identifying the instruction as a privileged instruction;

a first operand, for specifying the control register as a register to be modified; and

a second operand, for specifying a location of a second register within the microprocessor, said second register containing a bit mask, said bit mask determining which of the bit fields within the control register are to be modified;

wherein said bit mask is used to set or clear the bit fields in the control register;

whereby the bit fields in the control register are modified atomically by the privileged instruction.

21. (Original) The computer program product group as recited in claim 20 wherein the privileged instruction is executed when the microprocessor receives an interrupt signal.

22. (Original) The computer program product group as recited in claim 20 wherein the privileged instruction clears bit fields in the control register pertaining to corresponding bits that are set in said bit mask.

23. (Original) A computer data signal embodied in a transmission medium comprising:

computer-readable first program code for providing a bit clear instruction for execution on a microprocessor having a privileged control register, the bit clear instruction executing on the microprocessor when the microprocessor receives an interrupt and when the microprocessor is in a privileged state, said first program code comprising:

program code for providing a plurality of opcode bits for designating the bit clear instruction as a privileged instruction;

program code for providing a plurality of first operand bits for designating the privileged control register as the register to be operated upon by the bit clear instruction; and

program code for providing a plurality of second operand bits for designating a general purpose register as a register containing a bit mask, said bit mask specifying which of a plurality of bits within the privileged control register are to be cleared;

wherein when the bit clear instruction executes on the microprocessor, the plurality of bits within the privileged control register that are specified by said bit mask are cleared, atomically.